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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,204	03/29/2004	Kie Y. Ahn	500466.04 (29356/US/3)	5118

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EXAMINER	
SANTIAGO, MARICELI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,204	AHN ET AL.	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *62-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *62-96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Amendment, filed on August 9, 2004, has been entered and acknowledged by the Examiner.

Cancellation of claims 1-61 has been entered.

Claims 62-96 are pending in the instant application.

Specification

The current status of all nonprovisional parent applications referenced should be included. Reference to prior art applications should be updated to recite "This application is a continuation of United States Patent Application No. 09/994,511, filed on November 26, 2001, **now U.S. Patent No.** 6,835,111..."

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 62-69, 71-82 and 84-95 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 16-1-3, 7, 9 and 11-22 of

U.S. Patent No. 6,835,111. Although the conflicting claims are not identical, they are not patentably distinct from each other for the following similarities.

U.S. Application SN 10/813,204	U.S. Patent No. 6.835,111
Claim 62 recites a method of fabricating a porous dielectric layer in a field emission display comprising forming a polycrystalline silicon layer on a substrate and a plurality of columns on the substrate; forming pores in the polycrystalline silicon layer to form a porous polycrystalline silicon layer; and oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer.	Claim 16 states a method of fabricating a field emission display baseplate comprising forming columns on a substrate, forming a layer of silicon on the columns and the substrate, etching the silicon layer by anodizing a polycrystalline silicon layer to form a layer of porous polycrystalline silicon, and oxidizing the porous silicon layer to form a layer of porous silicon dioxide.
Claim 63 recites a method wherein the act of forming pores in the polycrystalline silicon layer comprises anodizing the polycrystalline silicon layer.	Claim 16 states a step of etching the silicon layer by anodizing a polycrystalline silicon layer to form a layer of porous polycrystalline silicon.
Claim 64 recites a method wherein the act of anodizing the polycrystalline silicon layer forms a porous polycrystalline silicon layer having at least 50% voids and the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.	Claim 17 states a method wherein the act of anodizing the polycrystalline silicon layer forms a porous polycrystalline silicon layer having at least 50% voids and the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.
Claim 65 recites a method wherein the act of anodizing the polycrystalline silicon layer forms a porous polycrystalline silicon layer having at least 75% voids and the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 61.5 % voids.	Claim 19 states a method wherein the act of anodizing the polycrystalline silicon layer forms a porous polycrystalline silicon layer having at least 75% voids and the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 61.5 % voids.
Claim 66 recites a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 3.	Claim 2 states a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 3.
Claim 67 recites a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 1.6.	Claim 3 states a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 1.6.
Claim 68 recites a method wherein the porous silicon dioxide layer is comprised of columnar silicon dioxide spacers with pores between the columnar spacers.	Claim 22 states a method wherein the porous silicon dioxide layer is comprised of columnar silicon dioxide spacers with pores between the columnar spacers.
Claim 69 recites a method further comprising planarizing the porous silicon dioxide layer.	Claim 16 states a method further comprising planarizing the porous silicon dioxide layer.
Claim 71 recites a method of fabricating a field emission display baseplate comprising	Claim 1 states a method of fabricating a field emission display baseplate comprising

forming columns on a substrate; forming a silicon layer on the columns and the substrate; etching the silicon layer to form a porous silicon layer, oxidizing the porous silicon layer to form a porous silicon dioxide layer, planarizing the porous silicon dioxide layer, forming an extraction grid on the porous silicon dioxide layer; etching openings through the porous silicon dioxide layer and the extraction grid; and forming emitters in the openings in the porous silicon dioxide and the extraction grid.	forming columns on a substrate; forming a silicon layer on the columns and the substrate; etching the silicon layer to form a porous silicon layer, oxidizing the porous silicon layer to form a porous silicon dioxide layer, planarizing the porous silicon dioxide layer, forming an extraction grid on the porous silicon dioxide layer; etching openings through the porous silicon dioxide layer and the extraction grid; and forming emitters in the openings in the porous silicon dioxide and the extraction grid.
Claim 72 recites a method wherein the act of etching the silicon layer forms a porous silicon layer having at least 50% voids and the act of oxidizing the porous silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.	Claim 9 states a method wherein the act of etching the silicon layer forms a porous silicon layer having at least 50% voids and the act of oxidizing the porous silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.
Claim 73 recites a method wherein the act of etching the silicon layer forms a porous silicon layer having at least 75% voids and the act of oxidizing the porous silicon layer forms a porous silicon dioxide layer having at least 61.5% voids.	Claim 7 states a method wherein the act of etching the silicon layer forms a porous silicon layer having at least 75% voids and the act of oxidizing the porous silicon layer forms a porous silicon dioxide layer having at least 61.5% voids.
Claim 74 recites a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 3.	Claim 2 states a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 3.
Claim 75 recites a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 1.6.	Claim 3 states a method wherein the act of oxidizing the porous polycrystalline silicon layer to provide a porous silicon dioxide layer comprises oxidizing the porous polycrystalline silicon layer to form a porous silicon dioxide layer having a relative dielectric constant of less than 1.6.
Claim 76 recites a method wherein the act of forming pores in the polycrystalline silicon layer comprises anodizing the polycrystalline silicon layer.	Claim 16 states a method wherein the act of forming pores in the polycrystalline silicon layer comprises anodizing the polycrystalline silicon layer.
Claim 77 recites a method wherein the act of forming emitters comprises forming a high resistance emitter body of silicon monoxide and metal.	Claim 11 states a method wherein the act of forming emitters comprises forming a high resistance emitter body of silicon monoxide and metal.
Claim 78 recites a method wherein the act of forming a high resistance emitter body comprises forming a high resistance emitter body by co-evaporation of silicon monoxide and a metal at an evaporation angle of 90 degrees with respect to the substrate surface.	Claim 12 states a method wherein the act of forming a high resistance emitter body comprises forming a high resistance emitter body by co-evaporation of silicon monoxide and a metal at an evaporation angle of 90 degrees with respect to the substrate surface.
Claim 79 recites a method further comprising, after the act of etching openings through the porous silicon dioxide layer and the extraction grid and	Claim 13 states a method further comprising, after the act of etching openings through the porous silicon dioxide layer and the extraction grid and

prior to the act of forming emitters in the openings in the porous silicon dioxide layer and the extraction grid, forming a sacrificial layer on the extraction grid by angle evaporation.	prior to the act of forming emitters in the openings in the porous silicon dioxide layer and the extraction grid, forming a sacrificial layer on the extraction grid by angle evaporation.
Claim 80 recites a method wherein the act of forming a sacrificial layer on the extraction grid by angle evaporation comprises forming a sacrificial layer on the extraction grid by angle evaporation at an angle of seventy five degrees or more from a surface normal of the substrate.	Claim 14 states a method wherein the act of forming a sacrificial layer on the extraction grid by angle evaporation comprises forming a sacrificial layer on the extraction grid by angle evaporation at an angle of seventy five degrees or more from a surface normal of the substrate.
Claim 81 recites a method wherein the act of forming emitters comprises forming emitter bodies by co-evaporating silicon monoxide and a metal, and forming emitter tips by evaporating a material having a work function of less than four electron volts.	Claim 15 states a method wherein the act of forming emitters comprises forming emitter bodies by co-evaporating silicon monoxide and a metal, and forming emitter tips by evaporating a material having a work function of less than four electron volts.
Claim 82 recites a method wherein the porous silicon dioxide layer is comprised of columnar silicon dioxide spacers with pores between the columnar spacers.	Claim 22 states a method wherein the porous silicon dioxide layer is comprised of columnar silicon dioxide spacers with pores between the columnar spacers.
Claim 84 recites a method of fabricating a field emission display baseplate comprising forming conductors on a substrate; forming a porous silicon dioxide layer on the conductors and on the substrate; planarizing the porous silicon dioxide layer; forming an extraction grid on the porous silicon dioxide layer; etching openings through the porous silicon dioxide layer and the extraction grid; and forming emitters in the openings in the porous silicon dioxide layer and the extraction grid.	Claim 1 states a method of fabricating a field emission display baseplate comprising forming conductors on a substrate; forming a porous silicon dioxide layer on the conductors and on the substrate; planarizing the porous silicon dioxide layer; forming an extraction grid on the porous silicon dioxide layer; etching openings through the porous silicon dioxide layer and the extraction grid; and forming emitters in the openings in the porous silicon dioxide layer and the extraction grid.
Claim 85 recites a method wherein the act of forming emitters comprises forming a high resistance emitter body of silicon monoxide and metal.	Claim 11 states a method wherein the act of forming emitters comprises forming a high resistance emitter body of silicon monoxide and metal.
Claim 86 recites a method wherein the act of forming a high resistance emitter body comprises forming a high resistance emitter body by co-evaporation of silicon monoxide and a metal at an evaporation angle of 90 degrees with respect to the substrate surface.	Claim 12 states a method wherein the act of forming a high resistance emitter body comprises forming a high resistance emitter body by co-evaporation of silicon monoxide and a metal at an evaporation angle of 90 degrees with respect to the substrate surface.
Claim 87 recites a method further comprising, after the act of etching openings through the porous silicon dioxide layer and the extraction grid and prior to the act of forming emitters in the openings in the porous silicon dioxide layer and the extraction grid, forming a sacrificial layer on the extraction grid by angle evaporation.	Claim 13 states a method further comprising, after the act of etching openings through the porous silicon dioxide layer and the extraction grid and prior to the act of forming emitters in the openings in the porous silicon dioxide layer and the extraction grid, forming a sacrificial layer on the extraction grid by angle evaporation.
Claim 88 recites a method wherein the act of forming a sacrificial layer on the extraction grid by	Claim 14 states a method wherein the act of forming a sacrificial layer on the extraction grid by

angle evaporation comprises forming a sacrificial layer on the extraction grid by angle evaporation at an angle of seventy five degrees or more from a surface normal of the substrate.	angle evaporation comprises forming a sacrificial layer on the extraction grid by angle evaporation at an angle of seventy five degrees or more from a surface normal of the substrate.
Claim 89 recites a method wherein the act of forming emitters comprises forming emitter bodies by co-evaporating silicon monoxide and a metal, and forming emitter tips by evaporating a material having a work function of less than four electron volts.	Claim 15 states a method wherein the act of forming emitters comprises forming emitter bodies by co-evaporating silicon monoxide and a metal, and forming emitter tips by evaporating a material having a work function of less than four electron volts.
Claim 90 recites a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon dioxide layer having a dielectric constant of less than 3.	Claim 18 states a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon dioxide layer having a dielectric constant of less than 3.
Claim 91 recites a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon dioxide layer having a dielectric constant of less than 1.6.	Claim 20 states a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon dioxide layer having a dielectric constant of less than 1.6.
Claim 92 recites a method wherein the porous silicon dioxide layer is comprised of columnar silicon dioxide spacers with pores between the columnar spacers.	Claim 22 states a method wherein the porous silicon dioxide layer is comprised of columnar silicon dioxide spacers with pores between the columnar spacers.
Claim 93 recites a method wherein the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.	Claim 17 states a method wherein the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 22.5% voids.
Claim 94 recites a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon dioxide layer having a dielectric constant of less than 3.	Claim 18 states a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon dioxide layer having a dielectric constant of less than 3.
Claim 95 recites a method wherein the act of forming a porous silicon dioxide layer comprises forming a porous silicon layer having at least 61.5% voids.	Claim 19 states a method wherein the act of oxidizing the porous polycrystalline silicon layer forms a porous silicon dioxide layer having at least 61.5 % voids.

Claims 70, 83 and 96 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 16 of U.S. Patent No. 6,835,111 in view of Jones et al. (US 5,647,785).

Claims 1 and 16 of Patent '111 fail to state the limitation of the act of planarizing the porous silicon dioxide layer comprises chemical-mechanical polishing the porous silicon dioxide layer as set forth in claims 70, 83 and 96. However, Jones discloses the a method of fabricating a field emission display baseplate further comprising the step of chemical-mechanical polishing

to planarize the insulating silicon layer. Accordingly, one skilled in the art at the time the invention was made would contemplate the obvious use of the conventional chemical-mechanical polishing for planarization purposes, as evidenced by Jones, in the manufacture of field emission display baspeplates.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/24/05

Mariceli Santiago
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Art Unit 2879